Electronic Version
Stylesheet Version v1.1.1

[METHOD FOR FABRICATING A MOSFET AND REDUCING LINE WIDTH OF GATE STRUCTURE]

Abstract

A method for fabricating a MOSFET is provided. The method comprises: providing a substrate, the substrate having a gate structure; forming a drain region and a source region in the substrate, the drain region and the source region being on two sides of the gate structure respectively; forming a metal silicide layer on the surface of the gate structure, the drain region, and the source region; forming a patterned block on the metal silicide layer above the gate structure, and forming a first dielectric layer above the substrate except the gate strcutre, the patterned block being formed above the center of the gate structure and the metal silicide layer above the gate structure beside two sides of the patterned block being exposed; removing a portion of the metal silicide layer and a portion of the gate structure by using the patterned block as a mask; and forming a drain extension region and a source extension region in the substrate, beside two sides of the remaining gate structure.